In the Specification:

Please amend the title as follows.

~~Non-destructive Evaluation of Microstructure and Interface Roughness of Electrically Conducting Lines in Semiconductor Integrated Circuits in Deep Sub-micron Regime~~ DETERMINATION OF GRAIN SIZES OF ELECTRICALLY CONDUCTIVE LINES IN SEMICONDUCTOR INTEGRATED CIRCUITS

Please amend paragraph 13 as follows.

FIGs. 1A-1D ~~1C~~ show a structure and a method for determining (a) line grain boundary electrical resistance R_b, (b) line geometry adjustment ε due to grain boundary electrical resistance for a line fabrication process and (c) the average grain size for a line width for the line fabrication process, in accordance with embodiments of the present invention.

Please amend paragraph 37 as follows.

In one embodiment, the above steps can be repeated for the other 10 different lines. The 11 lines have 11 different line widths. As a result, the average grain size of each particular line also represents the average grain size for the associated line width. Average grain size is one of the key parameters that need to be closely monitored during manufacturing process, interconnect research, and material development. FIG. 1D summarizes the steps of a method 900 for determining an average grain size. More specifically, in step 910, the line 110 (FIG. 1A) is formed having N sections of equal lengths. Next, in step 920, the resistances of the N sections are measured. Next, in step 930, the number of grains in the line 110 is determined. Next, in step 940, the average grain size of the line 110 is determined. Finally, in step 950, the average grain size is utilized in a manufacturing process, an interconnect research process, or a material

development process.